FIG.1

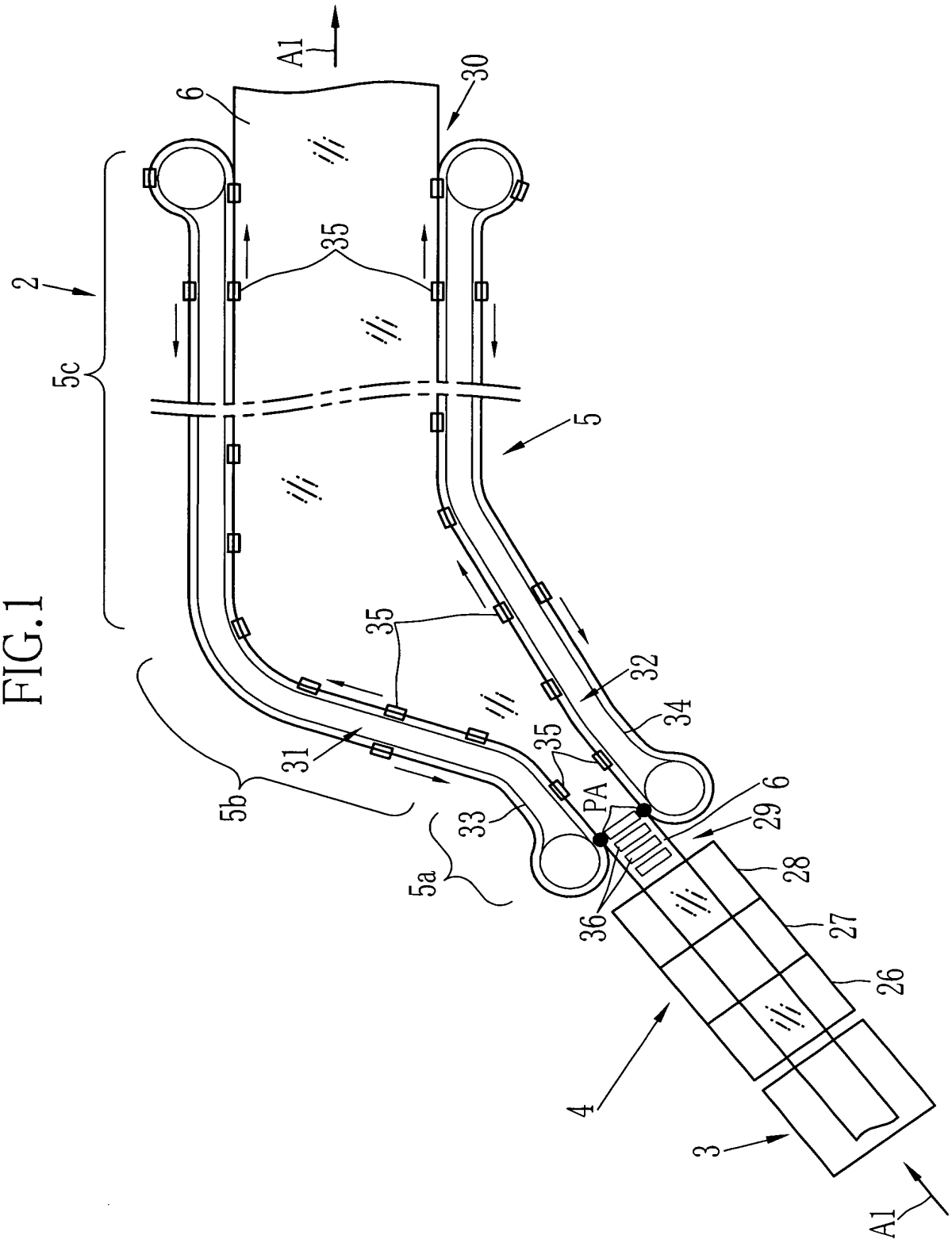


FIG.2

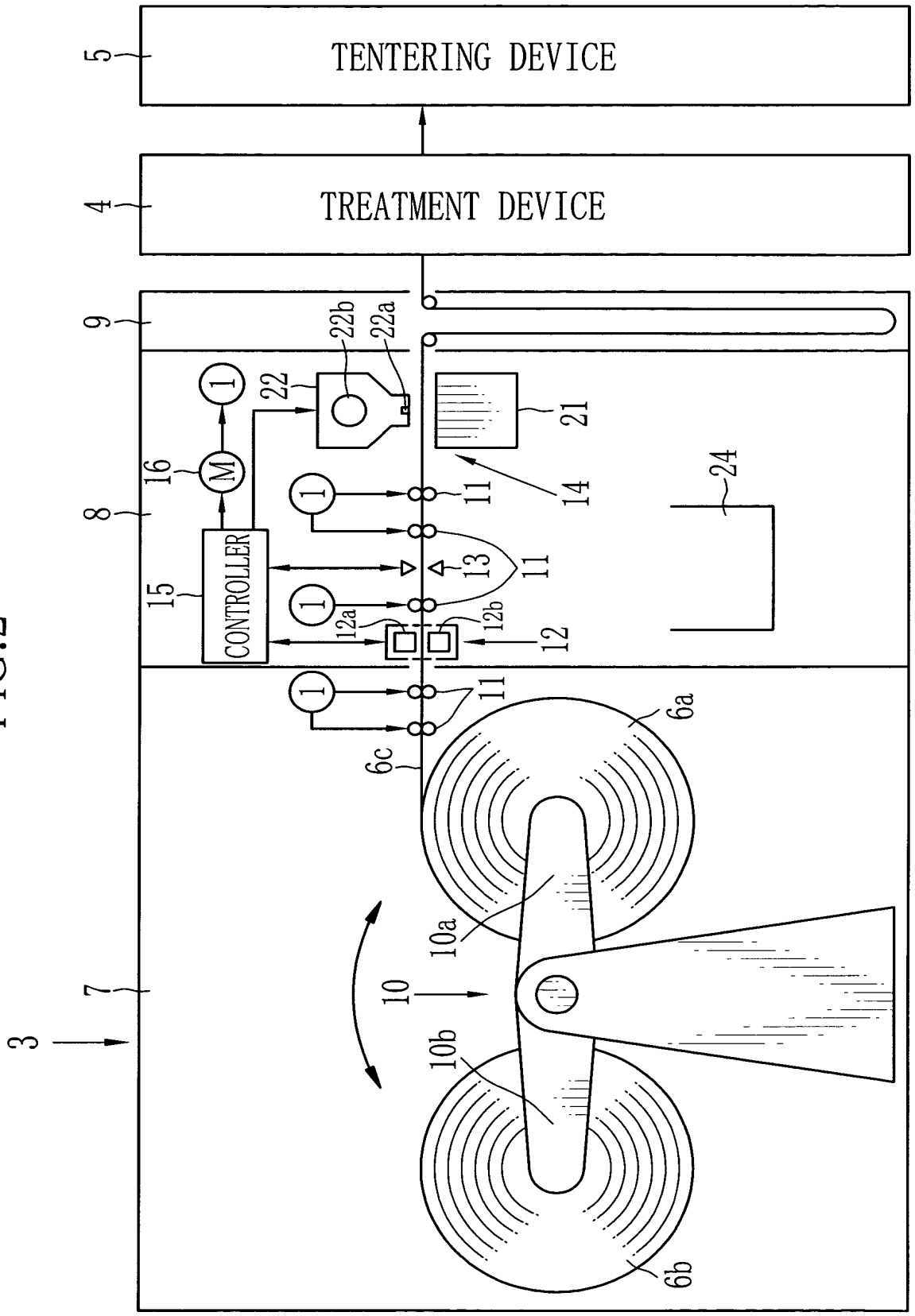

TENTERING DEVICE
TREATMENT DEVICE
CONTROLLER
M
1
3
4
5
6a
6b
6c
7
8
9
10
10a
10b
11
12
12a
12b
13
14
15
16
21
22
22a
22b
24

FIG.3

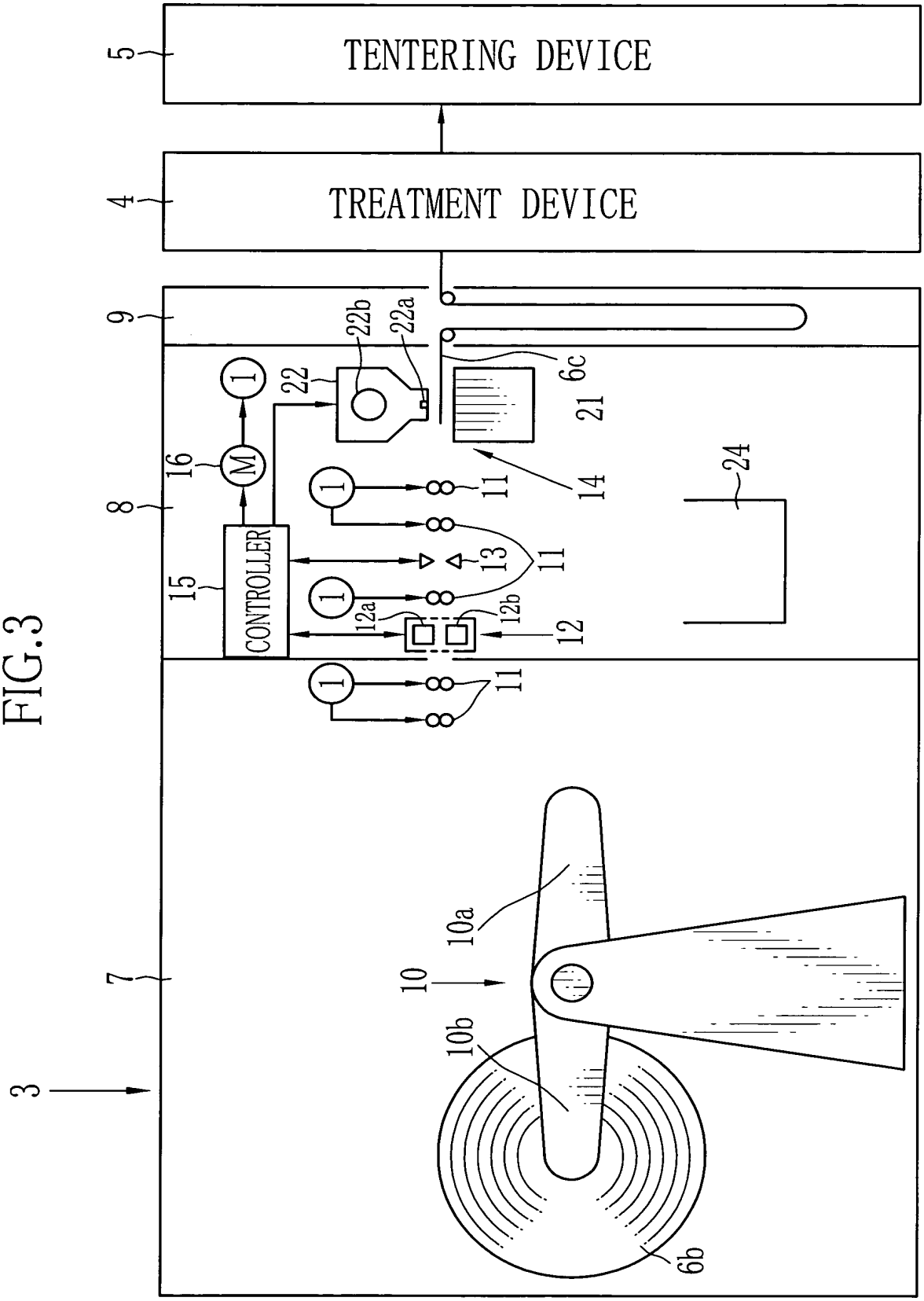

TENTERING DEVICE
TREATMENT DEVICE
CONTROLLER
M
1
3
4
5
6b
6c
7
8
9
10
10a
10b
11
12
12a
12b
13
14
15
16
21
22
22a
22b
24

FIG.4

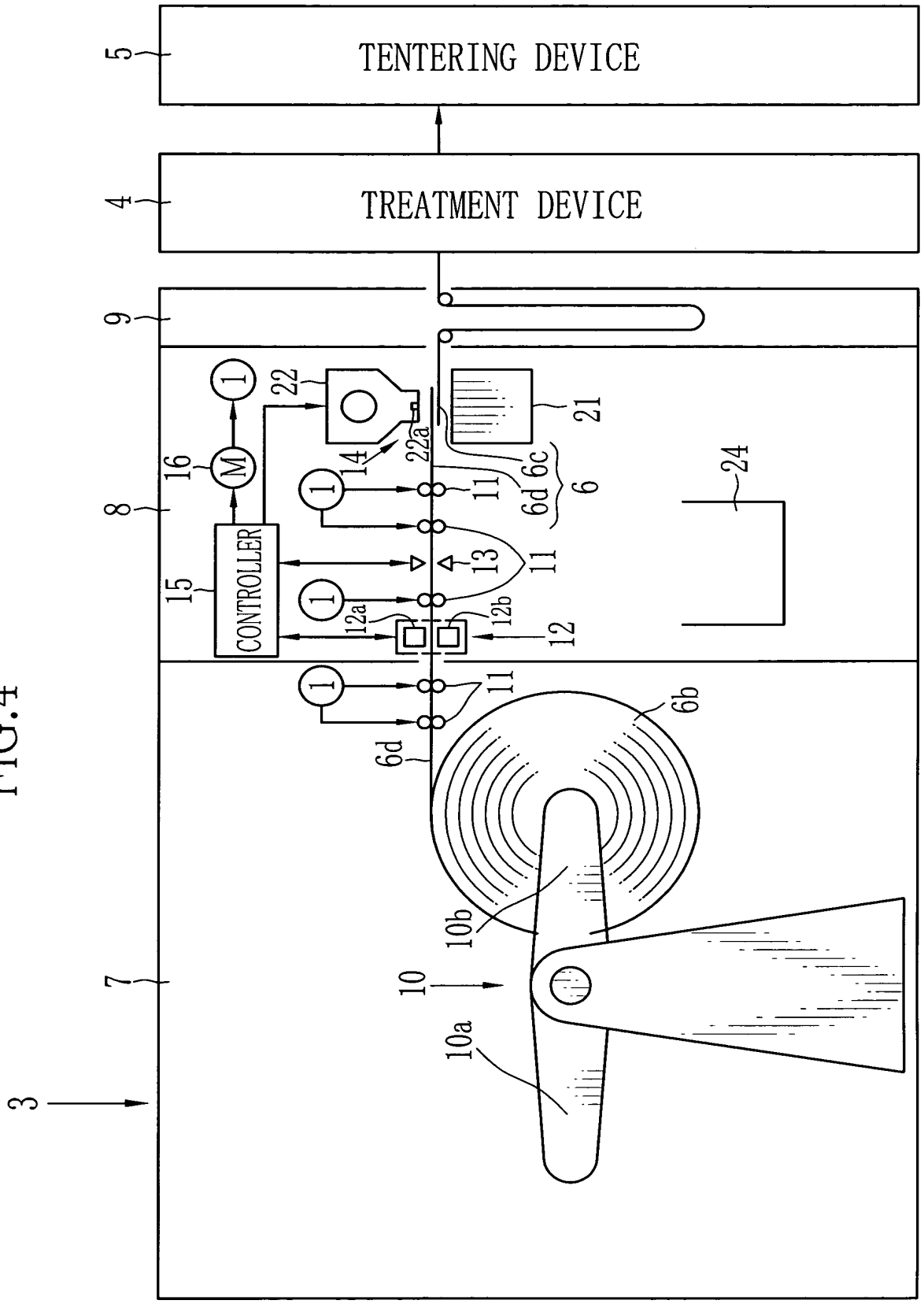

TENTERING DEVICE
TREATMENT DEVICE
CONTROLLER
M
1
3
4
5
6
6b
6c
6d
7
8
9
10
10a
10b
11
12
12a
12b
13
14
15
16
21
22
22a
24

FIG.5

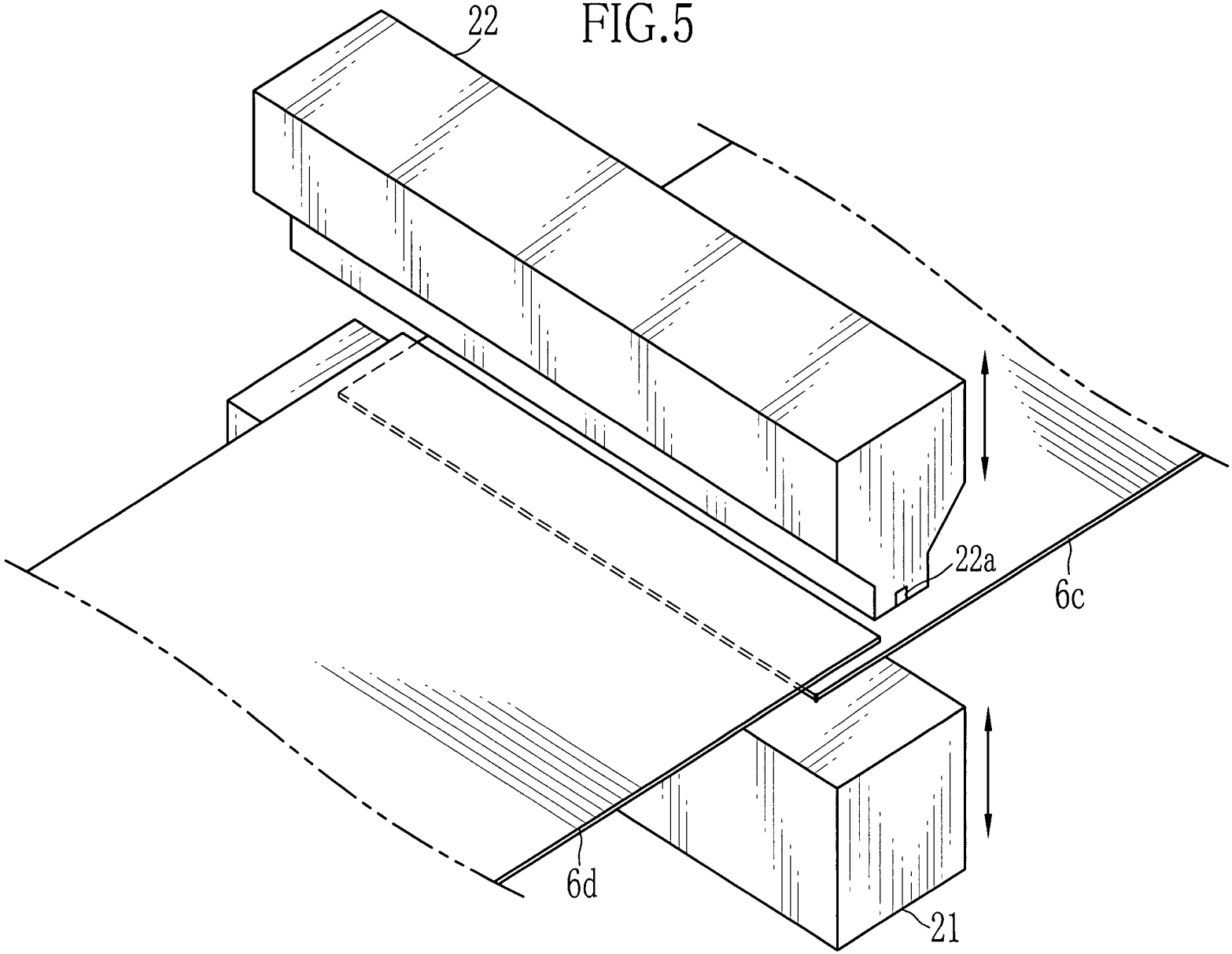


FIG.6B

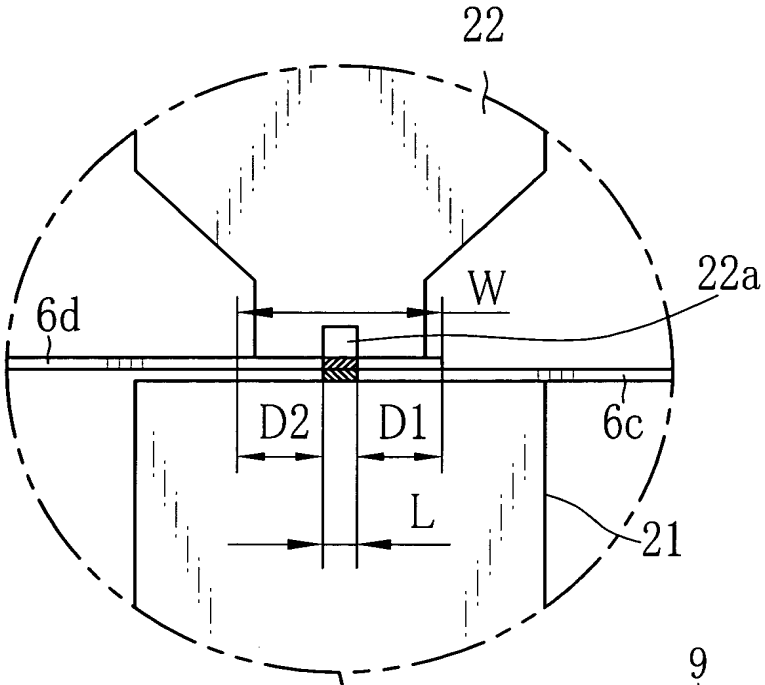

22
W
22a
6d
D2
D1
6c
L
21

FIG.6A

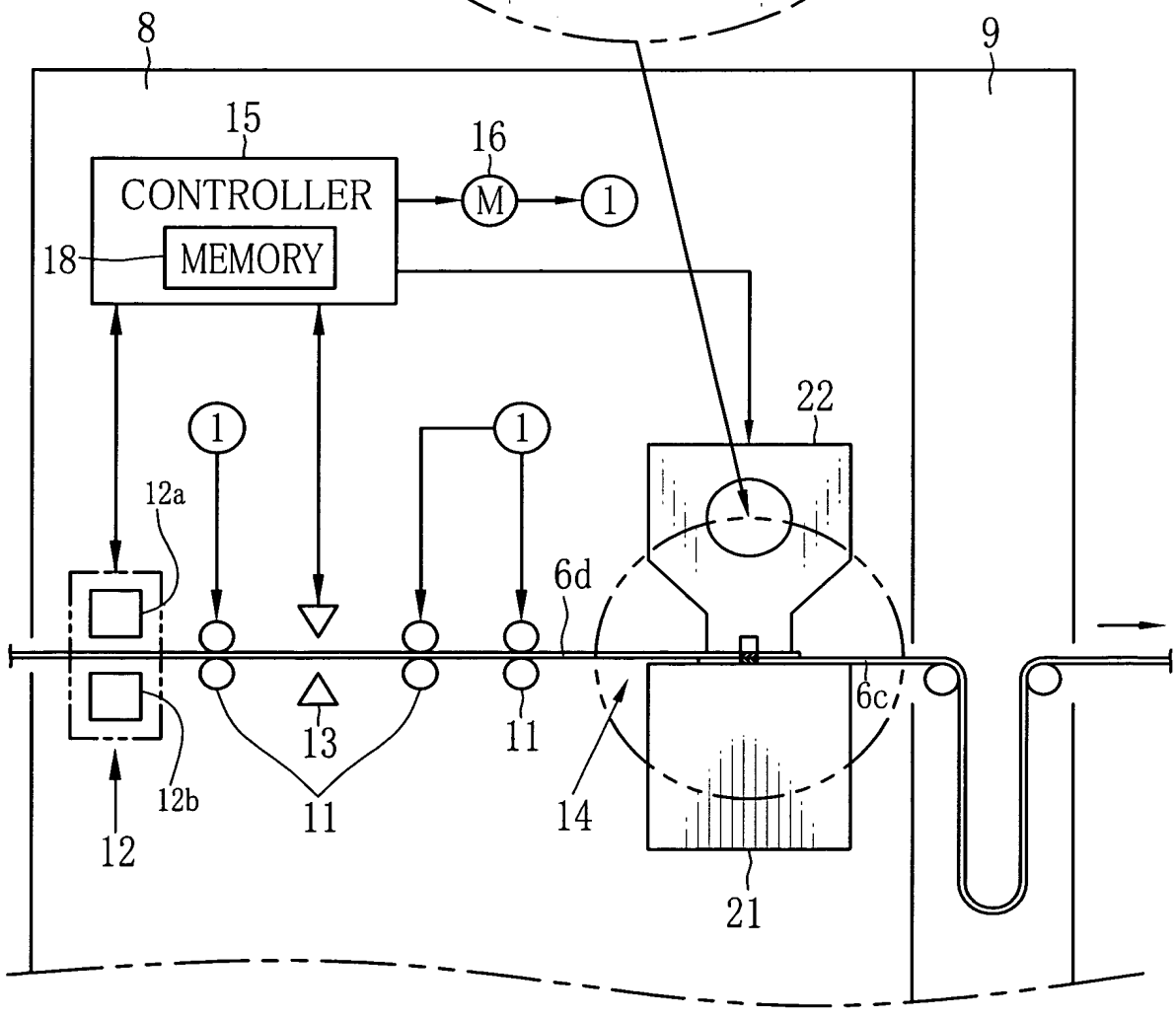

8
9
15
16
CONTROLLER
M
1
18
MEMORY
22
1
1
12a
6d
6c
13
11
11
14
12b
12
21

FIG.7B

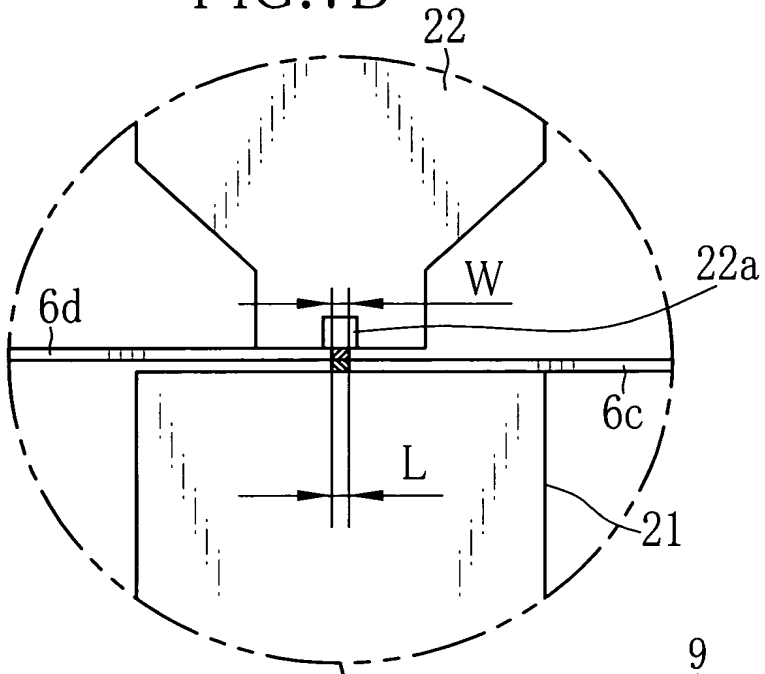
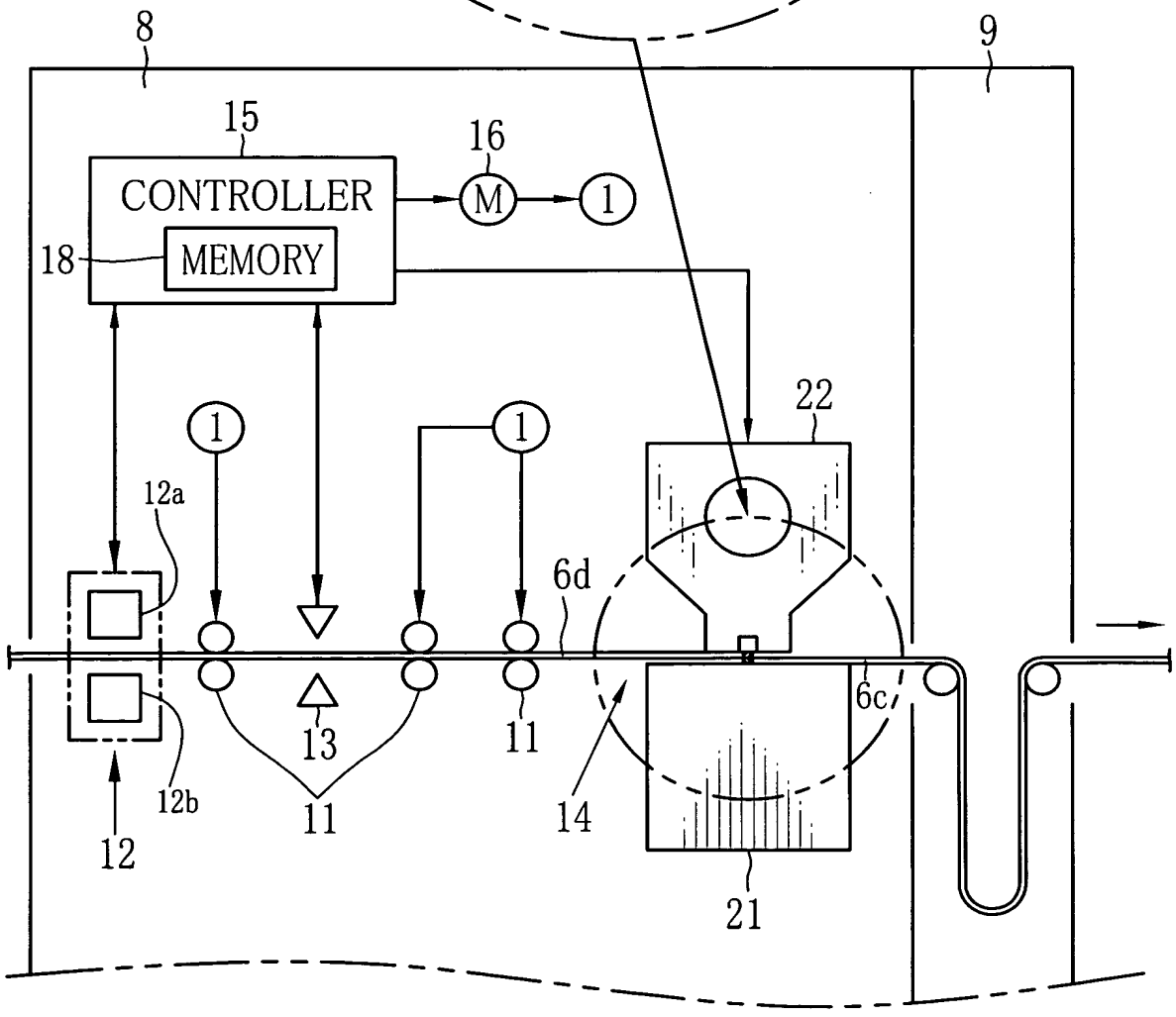

22
W
22a
6d
6c
L
21

FIG.7A


8
9
15
16
CONTROLLER
M
1
18
MEMORY
22
1
1
12a
6d
6c
13
11
11
14
12b
12
21